DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 8, 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura (US 2005/0025087) in view of Takahashi et al (US 2002/0105903) (see IDS).

(1) with regards to claims 1 and 8;

Tamura discloses in (figs. 1-4) a synchronization tracking (S21 and S22) apparatus and method comprising:

a replica generation section (fig. 1,16) that performs multicarrier demodulation of a known signal of a received signal (input from 15 and 17) and generates a replica (output to 12) (page 3, [0029]-[0031]);

a delay profile generation section (fig. 1, 12) that calculates a correlation value between said replica (16) and said received signal (Ich and Qch) and generates a delay profile (output of 12) (page 3, [0029]-[0035]);

a demodulation timing detection section (14) that detects demodulation timing at which multicarrier demodulation is performed from (page 3, [0032]).

Tamura discloses all of the subject matter disclosed above, but for specifically teaching

(a) an integral value calculation section that integrates said correlation values for each fixed range of said delay profile and calculates a plurality of integral values;

(b) a maximum integral value detection section that detects a maximum integral value which is a maximum value of said integral values;

(i) with regards to item (a) above;

However, Takahashi et al in the same endeavor (figs.7 and 8) discloses a synchronization tracking apparatus (see abstract) comprising: an integral value calculation section (fig. 8, (75-1) to (75-n)).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have incorporated the device of Takahashi et al Tamura in the system of Tamura in order to improve reception synchronization circuit for receiving data modulated by means of an OFDM technique (page 1, [0002]).

(ii) with regards to item (b) above;

However, Takahashi et al in the same endeavor (figs.7 and 8) discloses a synchronization tracking apparatus (see abstract) comprising: a maximum integral value detection section (fig.7, 176) (page 10, [0158]-[0159]);

an integral value calculation section (fig. 8, (75-1) to (75-n)) and

a maximum integral value detection section (fig.7, 176) (page 10, [0158]-[0159]);
It would have been obvious to one of ordinary skill in the art at the time of the invention to have incorporated the device of Takahashi et al Tamura in the system of Tamura in order to improve reception synchronization circuit for receiving data modulated by means of an OFDM technique (page 1, [0002]).

(2) with regards to claims 2 and 9;

Tamura discloses a first detection section that detects a first position at which said correlation value of said delay profile from said delay profile generation section first exceeds a threshold value from a start of said delay profile and generates first position information (fig. 4, page 4, [0047]-[0048]);

a second detection section that detects a second position at which said correlation value of said delay profile from said delay profile generation section first exceeds said threshold value from an end of said delay profile and generates second position information (fig. 4, page 4, [0049]-[0050]); and

an interval calculation section (fig. 2) that calculates an interval from said first position to said second position based on said first and second position information from said first and second detection sections and generates interval information and sends that interval information (page 4, [0037]-[0042]).

Tamura discloses correlation values for each fixed range of said delay profile from said delay profile generation section (fig. 1, 12).

Tamura discloses all of the subject matter disclosed above, but for specifically teaching

(a) an integral value calculation section that integrates said correlation values for each fixed range of said delay profile and calculates a plurality of integral values;

(b) a maximum integral value detection section that detects a maximum integral value which is a maximum value of said integral values;

(i) with regards to item (a) above;

However, Takahashi et al in the same endeavor (figs.7 and 8) discloses a synchronization tracking apparatus (see abstract) comprising: an integral value calculation section (fig. 8, (75-1) to (75-n)).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have incorporated the device of Takahashi et al Tamura in the system of Tamura in order to improve reception synchronization circuit for receiving data modulated by means of an OFDM technique (page 1, [0002]).

(ii) with regards to item (b) above;

However, Takahashi et al in the same endeavor (figs.7 and 8) discloses a synchronization tracking apparatus (see abstract) comprising: a maximum integral value detection section (fig.7, 176) (page 10, [0158]-[0159]);

It would have been obvious to one of ordinary skill in the art at the time of the invention to have incorporated the device of Takahashi et al Tamura in the system of Tamura in order to improve reception synchronization circuit for receiving data modulated by means of an OFDM technique (page 1, [0002]).

(3) with regards to claims 3 and 11;

Tamura further discloses said replica generation section (fig. 4, 16) performs multicarrier demodulation of a known signal of a plurality of received signals, generates a replica, and sends that replica to said delay profile generation section(fig. 4, 12) (page 3, [0029]-[0031]); and

said delay profile generation section (12) calculates a correlation value between said replica and said plurality of received signals and generates a plurality of delay profiles (fig. 4, 12 and page 3, [0031]);

Tamura discloses said synchronization tracking apparatus and method (figs. 3 and 4).

Tamura discloses all of the subject matter disclosed above, but for specifically teaching

(a) an integral value calculation section.

(b) an addition section that adds said plurality of delay profiles from said delay profile generation section and sends a result to said integral value calculation section.

(i) with regards to item (a);

However, Takahashi et al in the same endeavor (figs.7 and 8) discloses a synchronization tracking apparatus (see abstract) comprising: an integral value calculation section (fig. 8, (75-1) to (75-n)).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have incorporated the device of Takahashi et al Tamura in the system of Tamura in order to improve reception synchronization circuit for receiving data modulated by means of an OFDM technique (page 1, [0002]).

(ii) with regards to item (b) above;

However, Taguchi discloses in (fig.4), a plurality of delay profile circuits (9a-9c).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have incorporated the device of Taguchi in the circuit of Tamura as modified by Takahashi et al reduce power consumption when receiving signals.

3. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura (US 2005/0025087) in view of Takahashi et al (US 2002/0105903) as applied in claims 1 and 9 above, and further in view of Yamada et al (US 6980585).

(1) with regards to claims 4 and 12;

Tamura discloses wherein said replica generation section (fig. 4, 16) performs multicarrier demodulation of a known signal of a plurality of received signals, generates a replica, and sends that replica to said delay profile generation section (fig. 4, 12) (page 3, [0029]-[0031]);

wherein said synchronization tracking apparatus (figs.1, 3 and 4) further comprises wherein said delay profile generation section (fig. 4, 12) calculates a correlation value between said replica from said replica generation section and said received signal (fig. 4, 12) (page 3, [0029]-[0031]);

Tamura discloses all of the subject matter disclosed above, but for specifically teaching a selection section.

However, Yamada et al discloses a selection circuit (fig. 2, 50) that takes in two inputs and selects data corresponding to paths selected by the selecting path and from correlation circuit (co. 7, lines 6-10).

It would have been obvious to one of ordinary skilled in the art at the time the invention was made to have incorporated the device of Yamada et al in the system of Tamura as modified by Takahashi et al in order to provide a receiver circuit with a reduced scale (col.3, lines 45-47).

4. Claims 5 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura (US 2005/0025087) in view of Takahashi et al (US 2002/0105903) as applied in claims 1 and 9 above, and further in view of Okubo et al (US 20010033602).

(1) with regards to claims 5 and 13;

Tamura discloses wherein said delay profile generation section (fig. 1, 12) comprises:

a correlation value generation part (fig. 1, 12) that calculates a correlation value between said replica from said replica generation section (16) and said received signal (Ich and Qch)) ;

Tamura discloses all of the subject matter disclosed above, but for specifically teaching a thinning-out interval setting part that sets a thinning-out interval; and

an in-phase addition part that, when performing in-phase addition of said correlation values from said correlation value generation part, thins out correlation values at said thinning-out interval from said thinning-out interval setting part, performs correlation value in-phase addition, generates a correlation value, and sends that correlation value to said integral value calculation section.

However, Okubo et al discloses in fig. 5, in-phase correlation calculation section, (351), correlation signal calculation section (314) and in figs. 7 and 8 thinning-out interval setting part (page 6, [0075] and page 7, [0089], [0092]).

It would have been obvious to one of ordinary skilled in the art at the time the invention was made to have incorporated the device of Okubo et al in the system of Tamura as modified by Takahashi et al in order to improve bit error rate characteristic in demodulating data.

Allowable Subject Matter

5. Claims 14-20 are allowed.

The following is an examiner's statement of reasons for allowance: The prior art of record Tamura (US 2005/0025087) in view of Takahashi et al (US 2002/0105903) do not teach a synchronization tracking apparatus comprising:

a positive direction position detection section that detects a first position at which said correlation value first exceeds a threshold value in a positive direction which is a direction in which time advances from said maximum peak value in said fixed range in which said maximum integral value is calculated, and generates first position information;

a negative direction position detection section that detects a second position at which said correlation value first exceeds said threshold value in a negative direction which is a direction in which time is counted backward from said maximum peak value

in said fixed range in which said maximum integral value is calculated, and generates second position information;

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. Claims 6, 7 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record Tamura (US 2005/0025087) in view of Takahashi et al (US 2002/0105903) do not teach

a threshold value changing section that changes said threshold value and sends a resulting threshold value to said first and second detection sections when it is indicated by said determination result from said interval determination section that an interval is greater than or equal to said reference interval; and

another demodulation timing detection section that, when it is indicated by said determination result from said interval determination section that said interval is not greater than or equal to said reference interval, receives said first position information from said interval determination section and detects demodulation timing based on said first position of that first position information.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hasegawa et al (US 2004/0228272) discloses OFDM receiver method and OFDM receiver apparatus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HELENE TAYONG whose telephone number is (571)270-1675. The examiner can normally be reached on Monday-Friday 8:00 am to 5:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Liu Shuwang can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Helene Tayong/

Examiner, Art Unit 2611

June 20, 2008
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611